Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Claim 1 (previously canceled).

Claim 2 (previously amended). A static random access memory, wherein memory cells of the static random access memory each includes:

N-type MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other; and

P-type MOS transistors each having a channel-forming semiconductor region electrically connected with a power source,

wherein the channel-forming semiconductor regions of the P-type MOS transistors are formed of a same deep N-type well so that these channel-forming semiconductor regions are electrically connected to each other, and the channel-forming semiconductor regions of the N-type MOS transistors are formed of shallow P-type wells formed in the deep N-type well,

wherein trenches are individually provided between the channel-forming semiconductor regions of the P-type and N-type MOS transistors, said trenches being deeper than the shallow P-type wells, but shallower than the deep N-type well.

Claim 3 (original). A static random access memory as claimed in claim 2, wherein said P-type MOS transistor has a gate oxide film larger in thickness than said N-type MOS semiconductor transistor.

Claim 4 (previously canceled).

Claim 5 (previously amended). A static random access memory as claimed in claim 2, comprising write circuit means that include:

MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.

Claim 6 (original). A static random access memory as claimed in claim 5, wherein said MOS transistors of the write circuit means include N-type MOS transistors which serve to make a bit line and an inverted bit line have a high-level electric potential, respectively.

Claim 7 (previously amended). A static random access memory as claimed in claim 2, comprising read circuit means that include MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.

Claim 8 (previously canceled).

Claims 9-11 (canceled)

Claim 12 (new). A semiconductor device, comprising:

an inner region including an SRAM section and/or a logic circuit section, and having MOS transistors operating at a first voltage; and

an outer region including an interface section and located outside of the inner region, wherein

said interface section comprises first MOS transistors operating at the first voltage and second MOS transistors operating at a second voltage higher than the first voltage and performing direct signal transmission and reception to and from an external device

said first MOS transistors each have a channel-forming semiconductor region formed of a first well, and

said second MOS transistors each have a channel-forming semiconductor region formed of a second well deeper than the first well.